## Abstract of the Disclosure

An integrated circuit memory device includes a source line and a memory cell array that includes n memory cells that are connected to the source line. The n memory cells are operative to draw current from the source line in response to an n bit data word. A dummy memory cell circuit is operative to draw current from the source line responsive to the n bit data word such that a total current drawn by the memory cell array and the dummy memory cell circuit during a program operation is given by n * a current drawn by one of the n memory cells.